UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
RAMPURIA, SATISH

ART UNIT	PAPER NUMBER
2124	

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6

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>05 January 2001</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-4</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-4</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4)☐ Interview Summary (PTO-413) Paper No(s). _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION

1. Claims 1-4 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis

for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the
United States before the invention thereof by the applicant for patent, or on an international application
by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this
title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act

of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent

resulting directly or indirectly from an international application filed before

November 29, 2000. Therefore, the prior art date of the reference is determined

under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C.

102(e)).

3. Claims 1-2, and 4 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by

Cmelik et al (Cmelik), US Patent No. 6,031,992.

As per claim 1, Cmelik discloses:

- interpreting the source instructions by considering intent and purpose of the source

instructions (col. 2, 32-36 "the processor (interpreter) must be able to ensure that a primitive

instruction (source) which requires data resulting from another primitive instruction is run after

that other primitive instruction produces the needed (intended) data")

- translating interpreted source instructions to a set of equivalent operation code for

the target processor (col. 9, lines 29-30 "to translate a set of target instructions into instructions

of a host instruction set"). It is inherent that in translating the source code (target instructions), to

generate a host instruction set, a set of equivalent operation code must be generated in order to

ensure proper execution of the translated instructions on the host.

As per claim 2, Cmelik discloses:

- the interpreting step determines what the source instructions is trying to accomplish

and the optimum way of doing it at the target processor, in an "interpolative" and context

sensitive fashion (col. 12, lines 18-22 "translated instructions allows instructions to be recalled

without rerunning the lengthy process of determining which primitive instructions are required

(determine) to implement each target instruction "interpolative" and "context sensitive"") and

(col. 12, lines 24-25 "optimizing the sequence of primitive instructions").

As per claim 4, Cmelik discloses:

- a decoding stage for decoding the source instructions and parameters and creating an instruction stream that is optimized based on the source instructions and parameters (col. 5, lines 21-22 "The original target instructions are first decoded, and the sequence of primitive host instructions") and (col. 9, lines 54-56 "target instruction set to be translated, optimized, reordered, and rescheduled into very long instruction words (instruction stream)") and (col. 9, lines 60-61 "host instruction set which have been generated from a number of instructions (source) of the target instruction set")

- an optimization stage for optimizing flow of information and related operation code based on characteristics of the target processor (col. 12, lines 23-28 "optimizing the sequence of primitive instructions, allocating assets to each primitive instruction, reordering the primitive instructions, and executing each step of each sequence (flow of information) of primitive instructions involved each time each target instruction is executed"). It is inherent that instruction optimization is based on characteristics of the target processor, because the optimization is performed to enhance execution of instructions on the target processor.

- an encoding stage for encoding instructions specifically for the target processor to achieve the intended results, including further optimizing the operation code for the target processor (col. 9, lines 41-43 "means for updating state (intended) of the host computer from state of the target computer (processor)") and (col. 9, lines 54-56 "target instruction set to be translated, optimized, reordered, and rescheduled into very long instruction words")

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102
of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject
matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art
to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cmelik, US Patent No.

6,031,992 in view of Eaton et al (Eaton), US Patent No. 6,532,532.

As per claim 3, Cmelik discloses:

- the instructions that come before and after a current instruction to determine the

most efficient approach out of several available approaches for encoding the equivalent

operation code for the target processor to perform equivalent tasks specified by the source

instructions (col. 2, lines 27-31 "decodes each application instruction into a series of primitive

instructions so that those primitive instructions may be reordered and scheduled into the most

efficient execution order"), it is inherent that the process is done for target processor to perform

the similar task specified in the source instructions.

Cmelik does not explicitly disclose the translating step *processing the source instructions in*

blocks of varying sizes.

However, Eaton discloses processing source instructions in blocks of varying sizes to

optimize a translating stage (Abstract, "A computer system in which blocks of source code

instructions are translated into blocks of target code instructions and executed (processed)" and

"a block coalition mechanism selects blocks, and combines them to form an optimized

superblock of target code instructions" and "the system can start with relatively small, naively

translated blocks, and build up larger, more optimized blocks").

Therefore, it would have been obvious to a person of ordinary skill in the art

at the time the invention was made to incorporate the teaching of Eaton in to teaching of

Cmelik to process the source instructions in blocks of varying sizes to optimize the

translating stage in Cmelik disclosed system. The modification would be obvious because

of one of ordinary skill in the art would be motivated to provide opportunities for

eliminating redundant instructions within the target code block, and other optimizations

in Cmelik's disclosed system as suggested by Eaton in col. 1, lines 31-33.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure. A system is provided for a cross-compilation and emulation subsystem and

method for converting at run time, non-native code into native code immediately prior to

execution of that code as taught by Walters et al US Patent No. 5,768,593. Improving the

performance and optimizing compiler as taught by Hayashi et al US Patent No.

5,396,631. Method and apparatus for dynamically optimizing an executable computer

program as taught by Ravichandran, US Patent No. 6,085,029.

6. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Satish Rampuria whose telephone number is 703-305-

8891. The examiner can normally be reached on 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for

the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.

Satish Rampuria

Examiner

Art Unit 2124

12/09/03

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100